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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,263	06/25/2003	Manish Sharma	200300153-1	4523

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
HARRISON, MONICA D	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,263	SHARMA, MANISH	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/25/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 6-15, 17, 18, 22-24, 26, 27, 30-33, 35, 37 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Volfson et al (5,106,461).

1. Regarding claim 1, Volfson et al discloses a directional ion etching process for patterning self-aligned via contacts comprising: depositing a photoresist (Figure 3C, reference 213) on a patterned layer (Figure 3A, references 202, 204, 206); masking the photoresist to provide at least one protected area, the photoresist being developed to remove the photoresist from the non-protected area (column 7, lines 56-68); depositing a dielectric coating upon the patterned layer and the remaining photoresist (Figure 3E, reference 216), and ion etching at a low angle relative to the patterned layer to remove the dielectric coated photoresist, the removal of the photoresist thereby providing at least one self-aligned via contact (Figure 3E, references 222A and 222B; column 8, lines 1-16).

2. Regarding claim 3, Volfson et al discloses wherein ion etching is accomplished by a physically assisted process (column 8, lines 2-6; *RIE*).

3. Regarding claim 4, Volfson et al discloses wherein the physically assisted process is reactive ion etching (column 8, lines 2-6).

4. Regarding claim 6, Volfson et al discloses further including etching the patterned layer following the developing of the photoresist and prior to the depositing of the dielectric coating (Figure 3E, reference 214).

5. Regarding claim 7, Volfson et al discloses wherein the protected area is the intended location of at least one self-aligned via contact (Figure 3E, reference 222A).

6. Regarding claim 8, Volfson et al discloses wherein the dielectric coated photoresists extend substantially perpendicularly from the surface of the patterned layer, such that the low angle of ion etching relative to the patterned layer is a high angle relative to the extending coated photoresists (Figure 3E, reference 216).

7. Regarding claim 9, Volfson et al discloses wherein the via contact exposed by ion etching is in substantially the same plane as the remaining dielectric (Figure 3E, references 222A and 222B).

8. Regarding claim 10, Volfson et al discloses depositing an additional patterned layer and repeating the recited process to establish at least one additional self-aligned contact to the additional patterned layer (Figure 3F, references 224, 226 and 228).

9. Regarding claim 11, Volfson et al discloses wherein the additional patterned layer is a conductive layer (Figure 3F, references 224, 226 and 228; *chromium, copper,* and *titanium*).

10. Regarding claim 12, Volfson et al discloses directional ion etching process for patterning self-aligned via contacts, comprising: depositing a first conductive layer (Figure 3A, reference 202) on a wafer substrate (Figure 3A, reference 200); depositing a junction layer upon the first conductive layer, the junction layer being in electrical contact with the first conductive layer (Figure 3A, references 204 and 206); depositing a photoresist upon the junction layer

(Figure 3A, reference 208); masking the photoresist to provide a plurality of junction stacks, the photoresist being developed and the exposed junction layer being etched (Figure 3C, reference 213); depositing a dielectric coating upon the etching exposed surfaces and the photoresist (Figure 3E, reference 216); and ion etching at a low angle relative to the wafer substrate to remove the dielectric coated photoresist, the removal of the photoresist thereby providing at least one self-aligned via contact (column 8, lines 1-16).

11. Regarding claim 13, Volfson et al discloses depositing a first photoresist layer on the first conductive layer (Figure 3C, reference 213); masking the first photoresist layer to provide conductive rows, the photoresist being developed, the exposed conductive layer being etched and the remaining photoresist being dissolved to expose the conductive rows (Figure 3D, reference 214); depositing a first dielectric to insulate the conductive rows, the first dielectric being planarized to expose the top of the conductive rows before the junction layer is deposited. (Figure 3E, reference 216).

12. Regarding claim 14, Volfson et al discloses wherein the dielectric coating applied to the etching, exposed surfaces results in a surface substantially parallel to the wafer substrate, the coated photoresist extending substantially perpendicularly to the wafer substrate, such that the low angle of ion etching relative to the wafer substrate is a high angle relative to the extending coated photoresist (Figure 3E, reference 216).

13. Regarding claim 15, Volfson et al discloses wherein the via contact exposed by ion etching is in substantially the same plane as the surface substantially parallel to the wafer substrate (Figure 3F, reference 222A).

14. Regarding claim 17, Volfson et al discloses wherein the ion etching is accomplished by a physically assisted process (column 8, lines 2-6; *RIE*).

15. Regarding claim 18, Volfson et al discloses wherein the physically assisted process is reactive ion etching (column 8, lines 2-6).

16. Regarding claim 22, Volfson et al discloses depositing an additional patterned layer upon the exposed at least one via contact (Figure 3F, references 224, 226 and 228); depositing an additional photoresist on the additional patterned layer (Figure 3F, reference 232); masking the additional photoresist to provide at least one protected area, the additional photoresist being developed to remove the additional photoresist from the non-protected area (Figure 3G); depositing an additional dielectric coating upon the additional patterned layer and the remaining additional photoresist (Figure 3H, reference 240), and ion etching at a low angle relative to the additional patterned layer to remove the dielectric coated additional photoresist, the removal of the additional photoresist thereby providing at least one self-aligned via contact to the additional patterned layer (Figure 3H, references 236 and 238).

17. Regarding claim 23, Volfson et al discloses wherein the additional patterned layer is a conductive layer (Figure 3F, references 224, 226 and 228).

18. Regarding claim 24, Volfson et al discloses a directional ion etching process for patterning self-aligned via contacts comprising: depositing a first conductive layer Figure 3A, reference 202) upon a wafer substrate (Figure 3A, reference 200); depositing a first photoresist layer on the first conductive layer (Figure 3A, reference 208), masking the first photoresist layer to provide conductive rows, the photoresist being developed, the exposed conductive layer being etched and the remaining photoresist being dissolved to expose the conductive rows (Figure 3B,

reference 212); depositing a first dielectric to insulate the conductive rows, the first dielectric being planarized to expose the top of the conductive rows (Figure 3E, reference 216); depositing a junction layer upon the planarized dielectric, the junction layer being in electrical contact with the conductive rows (Figure 3F references 224, 226 and 228); depositing a second photoresist upon the junction layer (Figure3G, reference 232); masking the second photoresist to provide a plurality of junction stacks, the second photoresist being developed and the exposed junction layer being etched (Figure 3G), depositing a second dielectric to coat the etching exposed surfaces and the second photoresist (Figure 3H, reference 240) , and ion etching at a low angle relative to the wafer substrate to remove the dielectric coated second photoresist, the removal of the second photoresist thereby providing at least one self-aligned via contact (Figure 3H, references 238 and 236).

19. Regarding claim 26, Volfson et al discloses wherein the ion etching is accomplished by a physically assisted process (column 8, lines 2-6; *RIE*).

20. Regarding claim 27, Volfson et al discloses wherein the physically assisted process is reactive ion etching (column 8, lines 2-6).

21. Regarding claim 30, Volfson et al discloses wherein the first dielectric is planarized by CMP (column 4, lines 40-51).

22. Regarding claim 31, Volfson et al discloses wherein the second dielectric coating applied to the etching exposed surfaces results in a surface substantially parallel to the wafer substrate, the coated second photoresist extending substantially perpendicularly to the wafer substrate, such that the low angle of ion etching relative to the wafer substrate is a high angle relative to the extending coated second photoresist (Figure 3H, reference 240).

23. Regarding claim 32, Volfson et al discloses wherein the thickness of the second dielectric coating is substantially the height of the junction stacks, such that the top surface of the dielectric coating is in substantially the same plane as the top of the junction stacks (Figure 3H).

24. Regarding claim 33, Volfson et al discloses wherein the via contact exposed by ion etching is in substantially the same plane as the surface substantially parallel to the wafer substrate (Figure 3H, references 238 and 236).

25. Regarding claim 35, Volfson et al discloses depositing a second conductive layer upon the exposed via contacts (Figure 3I, references 242, 244 and 246), depositing a third photoresist layer on the second conductive layer (Figure 3J, reference 248); and masking the third photoresist layer to provide conductive columns transverse to the conductive rows, the third photoresist being developed, the exposed second conductive layer being etched and the remaining third photoresist being dissolved to expose the conductive columns (Figure 3J).

26. Regarding claim 37, Volfson et al discloses The process of claim 24, further including: depositing an additional patterned layer upon the exposed at least one via contact (Figure 3I references 242, 244 and 246), depositing an additional photoresist on the additional patterned layer (Figure 3J, reference 248); masking the additional photoresist to provide at least one protected area, the additional photoresist being developed to remove the additional photoresist from the non-protected area (Figure 3K); depositing an additional dielectric coating upon the additional patterned layer and the remaining additional photoresist (Figure 3K, reference 253), and ion etching at a low angle relative to the additional patterned layer to remove the dielectric coated additional photoresist, the removal of the additional photoresist thereby providing at least one self-aligned via contact to the additional patterned layer (Figure 3K).

27. Regarding claim 38, Volfson et al discloses wherein the additional patterned layer is a conductive layer (Figure 3I, references 242, 244 and 246).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 5, 16, 19-21, 25, 28, 29, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Volfson et al (5,106,461) in view of Gates et al (6,391,658 B2).

28. Volfson et al discloses all above claimed subject matter except physical ion etching (claims 2, 16 and 25), magnetic tunnel junction (claims 5, 19 and 28), ferromagnetic data (claim 20 and 29) and magnetic memory (claims 21, 34, and 36).

Gates et al discloses physical ion etching (column 8, lines 18-21; *ion beam etching*), magnetic tunnel junction (Figure 6A, reference 31'), ferromagnetic data (column 7, lines 47-53) and magnetic memory (column 2, lines 6-18).

Since Volfson et al and Gates et al are both from the same field of endeavor, the purpose discloses by Gates et al would have been recognized in the pertinent art of Volfson et al.

It is obvious, at the time the invention was made, for one with ordinary skill in the art, to modify Volfson et al with the teachings of Gates et al for the purpose of fabricating arrays of microelectronic elements such as magnetoresistive memory elements and FET's.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
March 18, 2005

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER